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Ternary Content Addressable Memory Types And Matchline Schemes

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Abstract
Ternary Content Addressable Memory (TCAM) used in many application like network routers and packet classification. To reduce the power consumption of matchlines, the matchline partitioning scheme is used. Matchline is partitioned into NOR and NAND type matchline. If NAND (NOR) type TCAM cell is used then NAND (NOR) type matchline is used. NOR type TCAM has feature of high speed and high compare power. NAND type TCAM has low speed and low compare power. The NAND and NOR type matchlines are combined to form the pai-sigma matchlines. In pai segment the NAND type cells are connected in parallel to form the NAND type matchline. In sigma segment NOR type cells are connected in series to form the NOR type matchline. When compare operation is performed all NAND type matchlines are activated because switching power is low. Based on the match result of the NAND matchlines the NOR matchlines are activated because of high speed. The matchline incurs the problem of short circuit current due to mismatch and match result of NAND and NOR matchlines. NAND type matchline exist the problem of charge sharing when the search result of the NAND line is mismatches. This proposed TCAM has less compare (search) power compared to the NAND/NOR type TCAM cell.

Key Words: Content Addressable Memories (CAM), Ternary CAM (TCAM), NAND TCAM, NOR TCAM, Matchline Power (MP), Ripple Precharge (RP), Internet Protocol (IP), Classless Inter-Domain Routing (CIDR), Match Line (ML).

I. INTRODUCTION

The ternary content addressable memory (TCAM) stores '0', '1' and 'x' bits. 'x' bit is called "don't care" or mask bit. High power dissipation is one of the major disadvantages of TCAM compared with random access memory (RAM) [8]. TCAM is one of the main devices in network routers and packet forwarding. TCAM can be classified into two types (1) NOR-type TCAM (2) NAND-type TCAM. NOR-type TCAM uses NOR-type matchlines and NAND-type uses NAND-type matchlines. Normally NOR-type TCAM has high search speed but at the increased cost of high power dissipation. NAND-type TCAM has low search speed with the advantage of low power dissipation.

A ternary symbol can be encoded into two bits [8]. These two bits are D and D' although these two bits are not necessarily complementary. These two bits can represent 4 states, but ternary storage requires three states only. SRAM cell is added to represent a ternary value. One bit connects to the left pull down path and its complementary bit connects to the right pull down path. By setting D and D' equal to logic '1' the bit 'x' will be stored in the TCAM, which disables both pull down paths and forces the cell to match regardless of the inputs. The logic '1' can be stored in the cell by setting bit D = 1 and D' = 0 and can store logic '0' by D = 0 and D'= 1. For searching the stored bit 'x' in the cells, set both SL and SL' to logic '0'.

The modification of ternary NOR-TCAM cell is shown in Fig.1 [12] by implementing the pull down transistors M_1-M_4 as PMOS devices and matchlines. The searchlines logic levels are complemented accordingly. By using PMOS devices the number of spacing between p-diffusion to n-diffusion in the cell and the wiring capacitance are reduced. Thus power consumption is less.

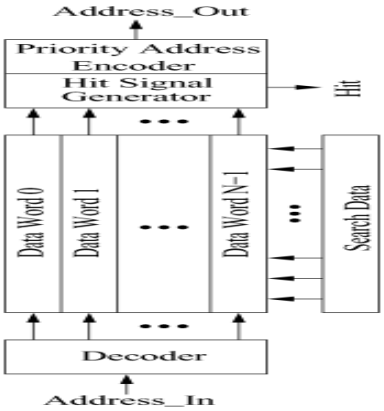

Fig -1: TCAM Architecture

The modification of ternary NAND-TCAM cell includes the mask bit at node M. the mask bit is set to

logic '0' to store 'x' in TCAM cell. This makes the mask transistor is 'ON' and shows always match regardless of the input bit D. For searching bit 'X' in the cell set both SL and SL to logic '1'. Fig 2. Shows the NOR and NAND type TCAM cells [12]. Both NAND and NOR type TCAM cell implements the XOR functions.

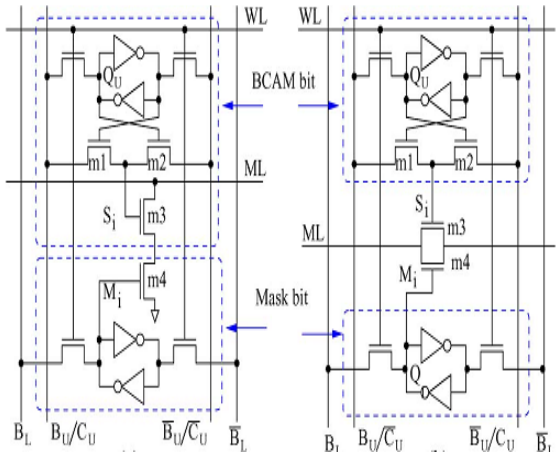

Fig -2: NOR and NAND type TCAM

Compare operation can be performed by prefetching data into comparand register and parallely compared with the symbols stored in the cell. Priority address encoder encodes highest priority matched address. Hit signal generator generates hit signal at the output if atleast one valid match. when TCAM executes compare operation the matchline (ML) 1 then ML value is determined by the comparison result of the upper BCAM bit.

II. MATCHLINE SCHEMES

Many low power design techniques where proposed a current-race sensing scheme [8] compares the stored data and search data through the NAND compare transistors. Ripple-precharge scheme is utilized for the longest prefix matching task. Prefix segregation scheme [5] is used in IP forwarding engine application.

Adaptive two-level tree style matchline scheme is used to reduce the power and improve the performance of the compare operation.

AND-type pseudo footless clock and data precharge dynamic gates with butterfly routing scheme to reduce the search time. Matchline partitioning scheme is used to reduce the power consumption of matchlines these are

a) Selective-precharge matchline scheme [1]

b) Matchline divided into two parts one is NAND-type TCAM and other one is NOR-type TCAM [5]

c) Pai – Sigma matchline scheme [12] to reduce compare power and short circuit current.

III. TYPES OF TERNARY CONTENT ADDRESSABLE MEMORIES (TCAM)

3.1 Hybrid Type TCAM

The hybrid-type TCAM [4] architecture has three different types of banks: the main bank, the sub-bank, and the extra bank. The main bank stores k–bit MF data out of *m*-bit data and the number of its word lines is equal to the number of sub-banks which store *m-k* bit IF data. The match result of each word line in the main bank is used to activate the corresponding sub-bank. If some data do not have any common MF with other data, the extra bank stores them without dividing them into Merged Field (MF) and Individual Field (IF).

Assuming that a B x *m* x *W* CAM of where is B the number of the banks, *m* is the bit width of a bank, and *W* is the number of words in a bank. Where is *k* the bit width. It is clear that the area of this architecture approximately becomes only *(m-k)/m* of the area of the conventional architecture, where k is the bit width.

3.2 Ripple Precharge TCAM

The structure of the Ripple-Precharge [7] CAM cell is shown in Figure 4. The main difference between the conventional TCAM cell and this cell is in the evaluation logic. The series NMOS transistors of the evaluation TCAM is replaced with PMOS transistors in the new CAM.

The source of the PMOS transistor is connected to IN_ML and its drain is connected to the drain of the discharging NMOS transistor whose source is grounded. The node which connects PMOS and the NMOS transistor is connected to the ML OUT line which is in turn connected to the ML IN line of the next bit. Therefore, the PMOS transistors in series ripple V_{dd} only when there is an exact match in the most significant four bits of the RP-TCAM word.

The additional NMOS transistor connected to the OUT_ML node of the parallel PMOS transistors ripples a '0' whenever there is a mismatch. The match line in the parallel part of the RP-TCAM is thus selectively charged by the rippling V_{dd} only when there is a match in the first 4 most significant bits. The behavior of the evaluation logic for a ripple-precharge [10] CAM cells is summarized in Table-I.

Table -1: Evaluation Logic of RP CAM

D	COMP	X	OUT_ML
0	0	0	V_{dd}
0	1	1	0
1	0	1	V_{dd}
1	1	0	0

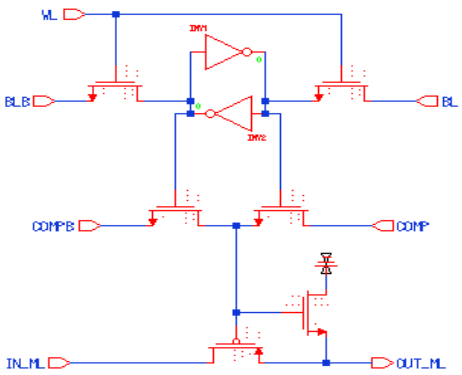

Fig -4: Structure of RP CAM

The RP-TCAM [7] architecture consists of both ripple precharge CAM bits and conventional TCAM bits. The first four most significant bits of the RP-TCAM word are intentionally CAM bits and not TCAM bits. This architectural change can be validated from the fact that most significant eight bits of the packet are never masked. Further, the elimination of mask bit from the first four most significant bits of the TCAM is justified from the results of packet profiling. This is mainly due to hierarchical structure of internet protocol (IP) address allocation in classless inter-domain routing (CIDR). Therefore, the first four most significant bits of the proposed 32-bit RP-TCAM word are CAM bits and the least significant twenty eight bits are TCAM bits. RP-TCAM architecture initially evaluates the first four most significant bits of the search key serially. If an exact match between the current data bit stored in the SRAM and the corresponding comparand bit sent through CMP and CMPB lines, the V_{dd} ripples through the current bit to evaluate the next bit. If a mismatch in any of the first four bits of the ripple-precharge CAM a "0" is propagated to the next bit from current mismatched bit. The match line in the second part is charged to V_{dd} only when there is a match in the first four CAM bits.

Whenever there is a mismatch in any one of the three most significant bits of the RP-TCAM, a "0" is propagated to the next bit. If this "0" starts to ripple through the subsequent bits i.e. considering subsequent bits to have an exact match, might end up having a V_t (threshold voltage) drop at match line (ML).

3.3 Mixed Serial-Parallel Scheme

A mixed serial-parallel CAM [3] (SPCAM) organization was implemented with the following design decisions based on the principles

- A mixed serial-parallel search method is used to minimize the transitions on the match lines.
- The search lines are separate from the bit lines and they are not forced to "0" or "1" while charging the match lines. The latter is accomplished by using a "virtual ground" line.
- The use of timing signals is minimized to reduce the energy consumed by their drivers.

Different CAM cells are used for the serial and parallel parts. The parallel CAM uses standard 10T cells with the ground connection of the two pull down nMOS chains testing the equivalence, replaced with $V_{gndMatch}$. This signal runs lengthwise and is connected to all the (parallel) CAM cells in the row. The four bits of the serial part are broken down into two sets of two bits to limit the maximum number of series transistors to three. The match signals of the two parts are ANDed together to produce the final result. SPCAM can operate either in serial or parallel mode. In serial mode, the four LSBs of each row are checked (serially) and, if they all match, the remaining bits are checked in parallel by pulling $V_{gndMatch}$ low. In parallel mode, both parts start matching at the same time; the four LSBs are still checked serially, but this operation is overlapped with the parallel matching of the second part.

In the serial part [3], a match propagates as a zero from the LSB to the most significant. A cell that matches opens its NMOS pass transistor, propagating the result from its less significant neighbor to its more significant neighbor. If it does not match, it breaks the chain and generates a one to pass on. If the first cell of a set does not match but the second does, a one is propagated through an NMOS transistor. This is allowed through only one device to minimize the speed loss. The gates at the output of these chains are designed so that their input threshold is lowered (with widened NMOS transistors) to compensate for the V_t voltage drop when their inputs are driven to high.

The precharge time should be made longer [8] so that the extra capacitance will be charged, or larger precharge transistors should be used that are able to charge the increased capacitance at the same time. If the LSBs match, $V_{gndMatch}$ will be pulled down. If the LSBs do not match, the final match line will stay low and the charging will continue, eventually reaching the appropriate level.

Serial (NAND-type) CAMs generally need timing signals in the cell array to control the precharging and evaluation of the match chains. In the operating mode of SPCAM, the initial intention was not to use timing signals at all. Unfortunately, a situation can occur which can only be overcome by using a timing signal: assume a search where, in some row, the LSBs all match but the MSBs mismatch. This will leave the row's parallel match line discharged.

IV. SINGLE PAI-SIGMA MATCHLINE SCHEME

Hybrid NAND-NOR matchline [12] is one favorite design approach to achieve the compromise between the power and delay of a matchline . When the CAM performs a compare operation, all the NAND matchlines are activated. But, only the NOR matchlines with the corresponding NAND matchlines generating a match result are activated. Since the switching power of the NAND matchline is low and only a small amount of NOR matchlines are activated, the compare power of the CAM with NAND-NOR matchlines can drastically be reduced. Also, the delay of the NAND-NOR matchline is better than that of the NAND matchline. The NAND/NOR matchline structure has the following major disadvantages: 1) the matchline incurs short circuit current (DC current) when the search results of the NAND matchline and the NOR matchline are match and miss, respectively, as shown in Fig. 5(a); 2) the NAND matchline may exist the problem of charge sharing when the search result of the NAND matchline is mismatch as shown in Fig. 5.b).

To reduce the short current, the pulsed NAND-NOR matchline [9] scheme uses a replica matchline. The replica matchline results in additional area cost and process variation will heavily degrade the effectiveness of short-current reduction. charge sharing can be eliminated by prechaging the searchlines to V_{dd} during the NAND matchline performs the precharge operation. There is additional power dissipation of search lines and the voltage of node S_i will be V_{dd} - V_t. If the search lines are precharged to V_{dd}, implies that the intermediate nodes of the NAND matchline can be precharged to V_{dd} - $2V_t$. Thus, the charge sharing issue still exists even if the search lines are precharged to for the typical NAND-type matchline.

The transistor-level diagram of the single Pai-Sigma matchline scheme is shown in Fig. 6, Where only the comparison logic of the TCAM cells is shown. The Pai segment realizes NAND function, The Sigma segment [12] realizes the NOR function. The Cellp-1 is merged with the interface logic between the Pai segment and Sigma segment. For the Pai segment, i.e., to, the comparison logic of each cell is comprised of two NMOS transistors in shunt and two PMOS transistors in series.

Each pair of PMOS and NMOS transistors is controlled by S_i and M_i. For the Sigma segment, i.e., to the comparison logic of each cell is two NMOS transistors in series. The comparison logic of the $Cell_{p-1}$ is mixed with the interface logic.

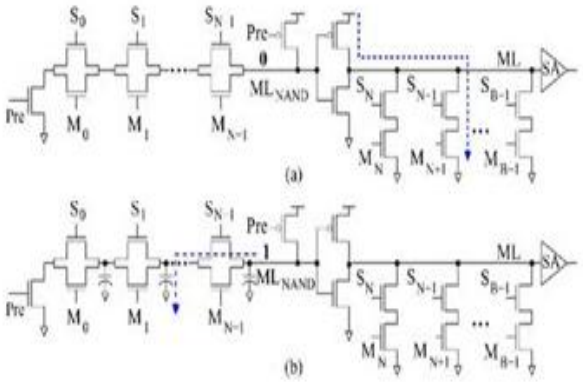

Fig -5: Short Current and Charge Sharing

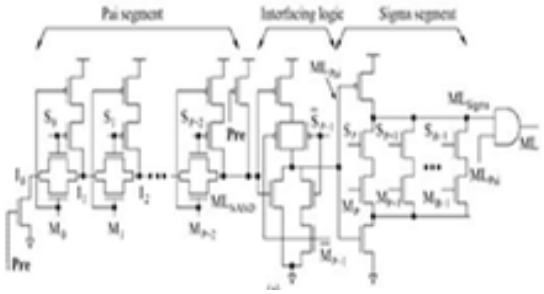

Fig -6: Pai-Sigma Matchline

V. PARALLEL PAI-SIGMA MATCHLINE SCHEME

The number of bits of the Pai matchline [12] has a great influence on the speed and power of the Compare operation. To design a low-energy TCAM, the product of the speed and power must be minimized. The product of the power and delay is minimal when the value of P is ranged from 8 to 10 for a 64-bit word. The delay contributed by the Pai segment can be reduced further by partitioning the Pai path into multiple Pai segments. For example, an 8-bit Pai segment can be implemented by 1, 2, 4, or 8 sub segments and then the comparison of those sub segments are evaluated by using interfacing logic circuits. The two-sub segment of the Pai segment has the lowest delay. Therefore, the two-sub segment of the Pai segment is selected to realize a Parallel Pai-Sigma matchline scheme (P^2SML). The Sigma segment is also partitioned into two sub segments to reduce the delay and power consumption.

Fig. 7 shows the proposed P^2SML scheme [12], where the Pai segment is separated into the PaiA and PaiB; and the Sigma segment is separated into the SigmaC and SigmaD. The precharge operation of the SigmaC and SigmaD is controlled by the result of ML_{Pai}. If the comparison result of the Pai segment is match, the ML_{Pai} = 0 and the matchlines of SigmaC and SigmaD are precharged to V_{dd}. The ML_{Pai} is the AND of ML_{PaiA} and ML_{PaiB}. If either ML_{PaiA} or ML_{PaiB} is at logic "0" (in precharge phase or a miss

result), then the ML_{Pai} is logic "0" and the matchlines of SigmaC and SigmaD can be precharged to V_{dd}. Therefore, only a precharge control circuit is implemented in the PaiA segment, which can guarantee the ML to be set to logic "0" in the precharge phase. This also reduce the power consumption contributed by the precharge signal.

If a Compare operation is performed, the precharge control signal Pre is set to 0 and the ML_{Pai} becomes logic '0'. Then, the matchlines of SigmaC and SigmaD are precharged to V_{dd} in the precharge phase. In the evaluation phase, if the comparison result of the Pai segment is match, then the ML_{PaiA} and ML_{PaiB} are logic 1. The state of ML_{Pai} thus becomes logic 1. Therefore, the NMOS transistors N1 and N2 are turned on and the matchlines of SigmaC and SigmaD are in the evaluation phase. If the comparison results of SigmaC and SigmaD are also match, then the results of the ML_{SigmaC} and ML_{SigmaD} are logic 1 and the ML is logic 1. If the comparison result of the Pai segment is mismatch, then the charge in the Sigma segment is not discharged, i.e., at logic 1 state.

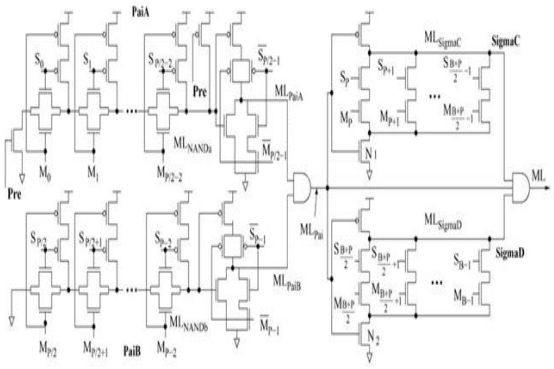

Fig -7:Parallel Pai-Sigma Matchline

VI. RESULT DISCUSSION

The NAND TCAM and NOR TCAM [12] simulation is shown in Fig. and Fig 8. Both type TCAM implements a XNOR function. When the input and the stored data matches ML discharges to ground. If not the ML will remain high.

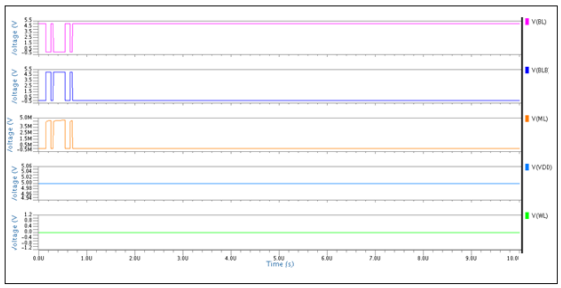

Fig -8: NAND Type TCAM

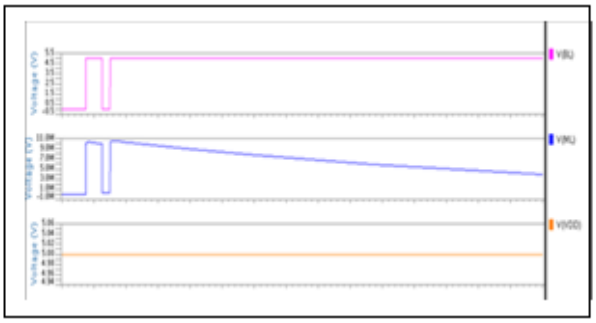

Fig -9: NOR Type TCAM

The pai-sigma matchline output will shown in Fig 10. The result will be for 8 bit operation. If all the bits are matched with the stored data the ML will discharges to ground. If not matched any one bit the ML remains high.

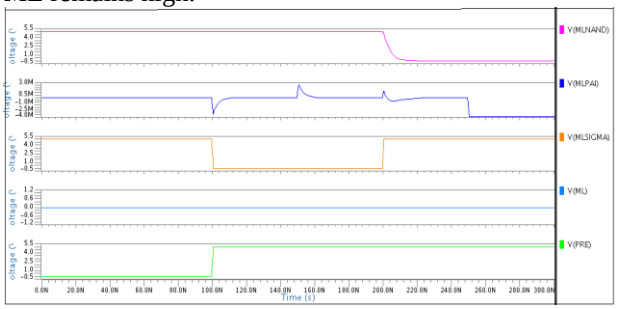

Fig -10: Pai-sigma matchline result

Initially all the matchlines are prechaged to high. When the comparison result of stored bit and the search bit will match, the precharged matchline will connected to ground by the pull down transistors. When the comparison result mismatches the precharged matchline will be in same state.

VII. CONCLUSION

In this paper we have presented CAM architecture and low power TCAM using the Pai-Sigma matchline scheme which does not incur the issues of charge sharing and the DC path. The switching activity of the search lines is also low. The power reduction can be achieved by precharging the internal nodes.

REFERENCES

[1]. C. A. Zukowski and S. Y. Wang, "*Use of selective precharge for low power content-addressable memories,"* in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), 1997, pp. 1788–1791.

[2]. I. Arsovski, T. Chandler, and A. Sheikholeslami, "*A ternary content addressable memory (TCAM) based on 4 T static storage and including a current-race sensing scheme*," IEEE J. Solid-State

Circuits, vol. 38, no. 1, pp. 155–158, Jan. 2003.

[3]. A. Efthymiou and J. D. Garside, "*A CAM with mixed serial-parallel comparison for use in low energy caches*," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 3, pp. 325–329, Mar. 2004.

[4]. S. Choi, K. Sohn, and H.-J. Yoo, "*A 0.7-fJ/bit/search 2.2-ns search time hybrid-type TCAM architecture*," IEEE J. Solid-State Circuits, vol. 40, no. 1, pp. 254–260, Jan. 2005.

[5]. M.-J. Akhbarizadeh, M. Nourani, and C. D. Cantrell, "*Prefix segregation scheme for a TCAM-based IP forwarding engine*," IEEE Micro, vol. 25, no. 4, pp. 48–63, Aug. 2005.

[6]. B.-D. Yang and L.-S. Kim, "*A low-power CAM using pulsed NAND-NOR match-line and charge-recycling search-line driver*," IEEE J. Solid-State Circuits, vol. 40, no. 8, pp. 1736–1744, Aug. 2005.

[7]. D. S. Vijayasarathi, M. Nourani, M. J. Akhbarizadeh, and P. T. Balsara, "*Ripple-precharge TCAM: A low-power solution for network search engines*," in Proc. IEEE Int. Conf. Comput. Design (ICCD), 2005, pp.243–248.

[8]. K. Pagiamtzis and A. Sheikholeslami, "*Content addressable memory (CAM) circuits and architectures:A tutorial and survey*," IEEE J. Solid- State Circuits, vol. 41, no. 3, pp. 712–727, Mar. 2006.

[9]. H.-Y. Li, C.-C. Chen, J.-S. Wang, and C.-W. Yeh, "*An AND-type match-line scheme for high-performance energy-efficient content addressable memories,"* IEEE J. Solid-State Circuits, vol. 41, no. 5, pp. 1108–1119, May 2006.

[10]. P.-T. Huang, S.-W. Chang, W.-Y. Liu, and W. Huang, "*A 256128 energy-efficient TCAM with novel low power schemes*," in Proc. IEEE Int. Symp. VLSI Design, Autom., Test (VLSI-DAT), 2007, pp. 1–4.

[11]. J.-S. Wang, C.-C. Wang, and C.-W. Yeh, "*High-speed and low-power design techniques for TCAM macros*," IEEE J. Solid-State Circuits, vol. 43, no. 2, pp. 530–540, Feb. 2008.

[12]. Shun-Hsun Yang, Yu-Jen Huang, and Jin-Fu Li, "*A Low-Power Ternary Content Addressable Memory With Pai-Sigma Matchlines*" IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 20, No. 10, October 2012.